

Article Info

Received: 01 Jan 2014 | Revised Submission: 20 Feb 2014 | Accepted: 28 Feb 2014 | Available Online: 15 Mar 2014

Protection of Power System Using Sequential Tripping

Mansi Kapoor, Jaikaran Singh**, Arvind Kumar Sharma***, Mayur Agarwal*****

ABSTRACT

This paper describes a Sequential Tripping Strategy used in an electrical power system to combat situations in which protection relays have maloperated or information is missing. This is an innovative back-up protection scheme designed to prevent the occurrence of widespread blackouts. It evaluates the certainty that transmission lines are likely to be affected by the fault and uses a Sequential Tripping Strategy to isolate the fault if a firm decision is not available due to maloperated relays and/or missing information. The mode of analysis and the Sequential Tripping Strategy ensures that the fault can be cleared at minimum risk to the network.

In applications like power stations and continuous process control plants, a protection system is used to trip faulty systems to prevent damages and ensure the overall safety of the personnel and machinery. But this often results in multiple or cascade tripping of a number of subunits. Looking at all the tripped units doesn't reveal the cause of failure. It is therefore very important to determine the sequence of events that have occurred in order to exactly trace out the cause of failure and revive the system with minimal loss of time.

Keywords: *Fault; Tripping, Power System Protection; etc.*

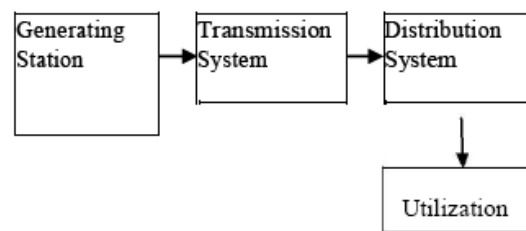
1.0 Introduction

1.1 Electrical power system

Electrical energy is produced through an energy conversion process. The electric power system is a network of interconnected components which generate electricity by converting different forms of energy to electrical energy and transmit to load centers to be used by the consumer. The production and transmission of electricity is relatively efficient and inexpensive. The electric power system consists of three main subsystems: the generation subsystem, the transmission subsystem, and the distribution subsystem. Electricity is generated at the generating station by converting a primary source of energy to electrical energy. The voltage output of the generators is then stepped-up to appropriate transmission levels using a step-up transformer. The transmission subsystem then transmits the power close to the load centers. The voltage is then stepped down to appropriate levels. The distribution subsystem then transmits the power close to the

customer where the voltage is stepped-down to appropriate levels for use by a residential, industrial, or commercial customer.

Fig 1: Block diagram of power system



Generated electricity is in the form of 3 phase supply which is step up in power substation. Then this high voltage electrical energy is transmitted by transmission lines over a long distance. Then it's stepped down in distribution substation to utilization level. This step up and step down is done by transformer. Then the electrical energy is distributed to different consumers.

*Corresponding Author: Department of Electrical Engineering, Mewar University, Chittorgarh, Rajasthan, India (E-mail: mayurag1@gmail.com)

**Department of Electrical Engineering, Mewar University, Chittorgarh, Rajasthan, India

***Department of Electrical Engineering, Mewar University, Chittorgarh, Rajasthan, India

****Department of Electrical Engineering, Mewar University, Chittorgarh, Rajasthan, India

1.2 Faults in electrical power systems

A fault occurs when two or more conductors that normally operate with a potential difference come in contact with each other. These faults may be caused by sudden failure of piece of equipment, by accidental damage or short circuit to overhead lines or by insulation failure resulting from lightning surges. Irrespective of the causes, the faults in 3 phase system can be classified into two main categories: Symmetrical faults, unsymmetrical faults, transient fault & persistent faults.

1.3 Power system protection

Power system protection is one of the several features of power system design. Every part of power system is protected. The factors affecting the choice of protection are type and rating of equipment, location of the equipment, types of faults, abnormal conditions and cost. The protective relaying is used to give alarm or to cause prompt removal of any element of power system from service when the element behaves abnormally.

The abnormal behavior of an element might cause damage or interference within effective operation of rest of the system. The protective scheme minimizes the damage to the equipment and interruptions to the service when electrical failure occurs.

The relays are compact and self contained devices which can sense abnormal conditions. Whenever abnormal conditions exist, the relay contacts get closed. This in turn closes trip circuit of circuit breaker. The circuit breakers are capable of disconnecting a faulty element, when they are called upon to do so by the relays.

Thus entire process includes the operations like occurrence of faults, operation of relay, opening of a circuit breaker and removal of faulty element. This entire process is automatic and fast, which is possible due to effective protective relaying scheme.

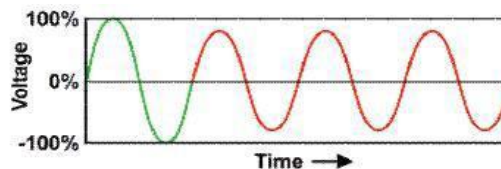
There are two principles for it. Firstly if the faults are not cleared quickly, it may cause unnecessary interruption of service to the customers. Secondly, rapid disconnection of faulted apparatus limits the amount of damage to it and prevents the effects of faults from spreading into the system.

2.0 Over/Under Voltage Protection

2.1 Under Voltage

Under voltage is classified as Long-duration Voltage Long-duration voltage variation is commonly defined as the root-mean-square (RMS) value deviations at power frequencies for longer than one (1) minute. It is important to note the duration of one minute or more as this differentiates under voltage from short-duration voltage variations such as voltage sags

Fig 2: Under Voltage Problem Waveform



Under voltage is described by IEEE 1159 as the decrease in the AC voltage (RMS), typically to 80% - 90% of nominal, at the power frequency for a period of time greater than 1 minute. Under voltage generally results from low distribution voltage because of heavily loaded circuits that lead to considerable voltage drop, switching on a large load or group of loads, or a capacitor bank switching off. For over and under voltage protection a simple solid state circuit is used which provides both under-voltage and over voltage protection to a household device.

Under voltage can expose electrical devices to problems such as overheating, malfunction, premature failure and shut down, especially for motors (i.e. refrigerators, dryers and air conditioners). Common symptoms of under voltage include: motors run hotter than normal and fail prematurely, dim incandescent lighting and batteries fail to recharge properly. In connection, IEEE discourages the use of the term "brownout" and should be avoided in future power quality activities to prevent confusion. Brownout is sometimes used to describe sustained periods of low power frequency voltage initiated as a specific utility dispatch strategy to reduce delivered power.

Basically, the disturbance described by brownout has the same meaning as that of under voltage. However, there is no formal definition for brownout and it is not as clear as the term under voltage. Under voltage problems may be alleviated by:

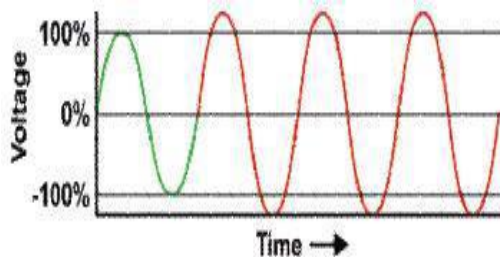
1. **Reducing the system impedance:** increase the size of the transformer, reduce the line length, add series capacitors or increase the size of line conductors.
2. **Improving the voltage profile:** adjust transformers to the correct tap setting (for manual tap changers) or install voltage regulators or automatic on-load tap changers. Voltage regulators include the mechanical tap changing voltage regulators, electronic tap switching voltage regulators and the ferroresonant transformers.
3. **Reducing the line current:** de-load the feeder or circuit by transferring some loads to other substations or load centers, add shunt capacitors or static VAR compensators, or upgrade the line to the next voltage level.

The choice of appropriate solution shall be based on the effectiveness of the mitigating device considering its benefit-cost factor.

2.2 Over voltage

Overvoltage is classified as a Long-duration Voltage Variation phenomenon, which is one of the general categories of power quality problems mentioned in the second post of the power quality basics series of this site. Long-duration voltage variation is commonly defined as the root-mean-square (RMS) value deviations at power frequencies for longer than one (1) minute.

Fig 3: Over voltage Waveform Overvoltage Protection Leads to Equipment Shutdown. Generally, Overvoltage can be Mitigated by:



Overvoltage protection leads to equipment shutdown. Generally, overvoltage can be mitigated by:

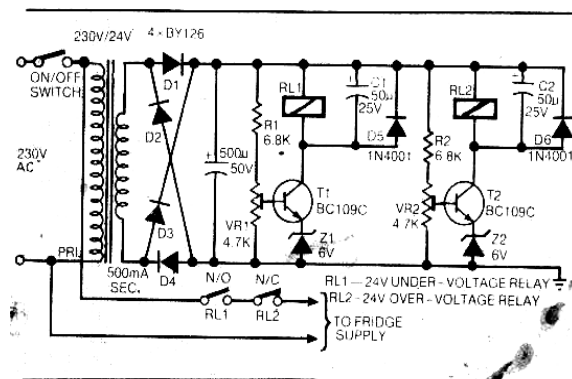
1. Adjusting transformers to the correct tap setting (for manual tap changers) or installing voltage regulators or automatic on-load tap changers to improve the voltage profile. Voltage regulators include the servo-mechanical tap switching voltage regulators, electronic tap switching voltage regulators and the ferroresonant transformers.
2. Manually or automatically switching off excess capacitor banks during light load or off peak hours.
3. The chosen solution shall be evaluated based on its effectiveness and with consideration to the benefits and costs.

3.0 Over/Under Voltage Protection

Various types of commercial stabilizers available in the market do not normally provide the cut-off at the extreme voltage limits, which is very important for devices. If the supply voltage varies within +10V, there is no harm done to a device. But protection is absolutely essential if the supply varies beyond these limits. The circuit described here cuts off the supply whenever it goes beyond the set limits.

The base voltage of transistor T1 should be adjusted to just over 6V with preset VR1 so that the under-voltage relay RL1 just gets energized at the normal voltage. This relay should get released at the lower voltage limit.

Fig 4: Circuit diagram for over/under voltage protection



At normal voltage, RL1 should remain energized. Similarly, the base voltage of T2 should be adjusted to just under 6V by the corresponding preset VR2 such that RL2 just gets energized at the upper voltage limit and is released at the normal voltage. Normally open contact (N/O) of RL1 normally-closed contact (N/C) of RL2 is connected in series with the supply.

A step down transformer is given supply of 230 V which steps it down to 24v. The supply is then passed to a bridge rectifier which rectifies the supply and converts it to a 24V d.c. Two relays are connected in series connection in which one is overvoltage relay and other is under voltage relay. Each relay has a variable resistor which can be adjusted for +10V. When the voltage decreases from the range of the under voltage relay the relay trips the circuit and the supply is closed. Similarly when the voltage increases from the range of over voltage relay the relay trips the circuit and the supply is again closed. In this way we can save the circuit from the over voltage and under voltage faults. This circuit can be used to protect power control stations for overload protection and the same can be interfaced with the PC or any microcontroller based automation circuits. The major components used in these are

- 3 capacitors (1x500uF, 50V;2x 50uF, 25V)
- 2xRelays (over voltage, under voltage)
- Resistances(2x6.8kΩ)
- 2x Zener Diodes(6V)
- Bridge rectifier
- Step down transformer(230V/24V)
- Transistors

4.0 Sequential Tripping

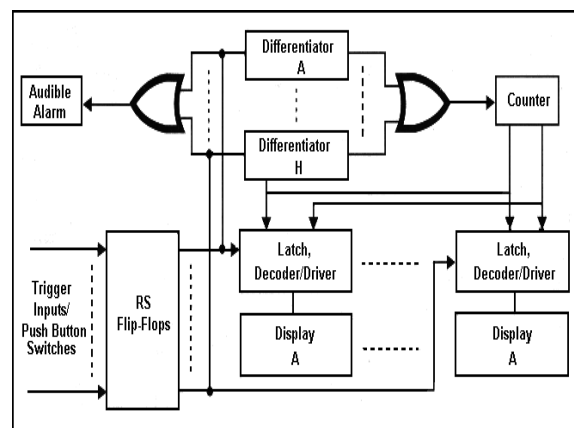
In applications like power stations and continuous process control plants, a protection system¹ is used to trip faulty systems to prevent damages and² ensure the overall safety of the personnel and machinery. But this often results in multiple or cascade tripping of a number of subunits. Looking at all the tripped units doesn't reveal the cause of failure³. It is therefore very important to determine the sequence of events that have occurred in order to exactly trace out the cause of failure and revive the system with minimal loss of time.

The circuit presented here stores the tripping sequence in a system with up to four units/blocks. It uses an auxiliary relay contact point in each unit that closes whenever tripping of the corresponding unit occurs. Such contact points can be identified easily, especially in systems using programmable logic controllers (PLCs).

The circuit records tripping of up to four units and displays the order in which they tripped. A clock circuit, however fast, cannot be employed in this circuit because the clock period it will be a limiting factor for sensing the incidence of fault. Besides, it may also mask a number of events that might have occurred during the period when the clock was low. Hence the events themselves are used as clock signals in this circuit.

Fig.5 shows the block diagram of the tripping sequence. The inputs derived from auxiliary relay contacts (N/O) of subunits or push-to-on switches are latched by RS flip-flop when the corresponding subunits trip, causing the following four actions:

Fig: 5. Block diagram of sequential tripping



The latch outputs are ordered to activate audio alarm. The latch outputs are differentiated individually and then ordered to provide clock pulses to the counter to increment the output of the counter that is initially preset at 1 (decimal). Each individual latch output activates the associated latch/decoder/driver and 7-segment display set to display the number held at the output of the counter, which, in fact, indicates the total number of trips that have taken place since the last presetting.

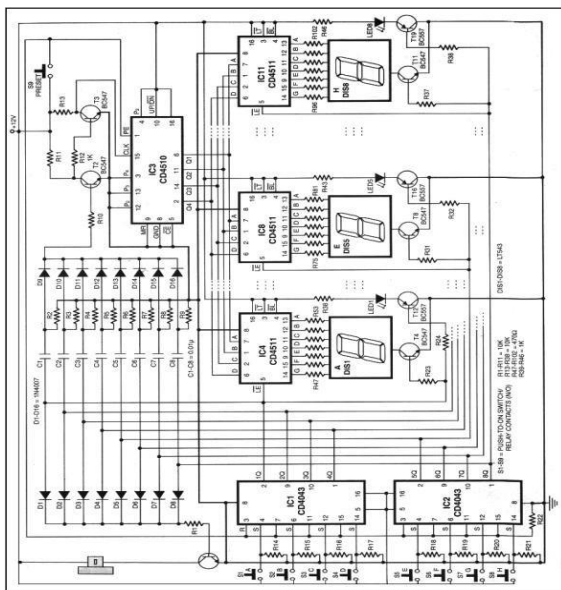
- LEDs associated with each of the latch, decoder, and driver sets remain lit to indicate the readiness of the sets to receive the tripping input. LEDs associated with the tripped unit go off.

5.0 The Circuit

IC1 and IC2 (CD4043) Quad NOR RS flip-flops in Fig.6 are used to capture and store the information pertaining to the tripping of individual units. Reset pins of all the four flip-flops and sub-parallel enable (PE) pin 1 of BCD up-/down-counter CD4510 (IC3) are returned to ground via 10-kilo-ohm resistor R22, while set pins of all RS flip-flops are returned to ground via individual 10-kilo-ohm resistors R14 through R21.

Initially, all the four Q outputs of IC1 and IC2 are at logic 0. The auxiliary relay contacts of the subunits, which are depicted here by push-to-on switches S1 through S4, connect the set terminal of the corresponding stage of RS flip-flop to +12V whenever tripping of a specific subunit occurs. This makes the output of the associated flip-flop go high. Thus whenever a sequence of tripping of subunits occurs, the corresponding outputs (1Q to 4Q) go high in the order of the tripping of the associated subunits.

Fig. 6. Circuit Diagram of Sequential Tripping



All the four Q outputs are connected to the corresponding latch-enable inputs of BCD latch-

cum- decoder-driver ICs (CD4511). These Q outputs are also ORed using diodes D1 through D8 to activate an audible alarm and also routed to a set of differentiator networks (comprising capacitors C1 through C8 and resistors R2 through R9).

A differentiator provides a sharp pulse corresponding to the tripping of a subunit. All such differentiated pulses are ORed via diodes D9 through D16 and coupled to the counter stage formed by IC3 (CD4510, a synchronous up-/down-counter with preset) after amplification and pulse shaping by transistor amplifier stages built around transistors T2 and T3.

These pulses serve as clock to count the number of tripping that occurred after a reset.

6.0 CD4043BC LATCH

The CD4043BC are quad cross-couple 3-STATE CMOS NOR latches. It has a Q output and SET and RESET inputs. There is a 3-STATE ENABLE input for all latches. Logic “1” on the ENABLE input connects the latch states to the Q outputs. Logic “0” on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The 3-STATE feature allows common bussing of the outputs.

7.0 CD4511BC

The CD4511BC BCD-to-seven segment latch/decoder/ driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure.

The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability.

Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

8.0 Operation Of Circuit

Let us assume that three units, say, C, D, and A (third, fourth, and first), tripped in that order following a fault. When the system is reset (before any tripping), the outputs of all RS flip-flops (1Q through 8Q) are low. This LE* active-low makes latches IC4 through IC11 transparent and as the counter is preset to 1 (since P1 input is high while P2, P3, and P4 are low) with the help of switch S9, all the latches hold that '1' and their decoded 'b' and 'c' segment outputs go high.

However, the common-cathode drive is absent in all the 7-segment displays because driver transistors T4 through T11 are cut off due to the low outputs of all RS flip-flops and hence the displays are blank. At the same time, the low outputs of all RS flip-flops (1Q through 4Q) forward bias PnP transistors T12 through T19 associated with LED1 through LED4 of each of the displays. As a result, all these LEDs glow, indicating no tripping. Now when unit C trips, output 3Q of RS flip-flop IC2 goes high to provide the base drive to common-cathode drive transistor T8. This, in turn, activates DIS5 to display '1', indicating that unit C tripped first.

The corresponding LED3 goes off as transistor T16 is cut off. Also, latch IC8 is disabled due to logic 1 on its pin 5 and therefore it does not respond to further changes in its BCD data input. The differentiator formed by C5 and R6 responds to the low-to-high transition of 5Q and generates a short pulse.

This pulse passes through diode D13 and transistors T2 and T3 and reaches clock pin of counter IC3. The counter counts up and its output becomes 0010 (decimal 2).

As mentioned earlier, all the display units other than C have the drive signal on segments a, b, g, e, and c now but are off because of the missing common-cathode drive. When the next subunit D trips, output 4Q experiences a low-to-high transition and the corresponding display (DIS4) shows digit '2'. The above sequence of operation holds true for any further subunit tripping-with the displayed digit incrementing by one for each sequential tripping. In the prototype, LEDs D17 through D24 were fixed below the corresponding 7-segment displays pertaining to subunits A through D to provide a visual indication that these units are ready to respond to a tripping.

The circuit works satisfactorily with twisted-pair wires of length up to 5-metres. In electrically noisy environments, the length of the cable has to be reduced or a shielded twisted-pair cable can be used. An actual-size, single-side PCB layout for the main control portion of the tripping sequence recorder-cum-indicator circuit is shown in figure-4.7 and its component layout. The indicator set of can be connected to the main PCB of using Berg strip type SIP (single-inline-pin) connectors as per requirements.

This tripping sequence recorder-cum-indicator circuit can also be used in quiz games to decide the order in which the teams responded to a common question. For this, provide push-to-on switches on the tables of individual teams and a master reset to the quiz master. Modify the alarm circuit suitably with a retrigger able monostable stage so that the audible alarm stops after a short interval.

Fig 7: Actual size, single side PCB of the Main Control Portion of Tripping Sequence Controller cum Indicating Circuit

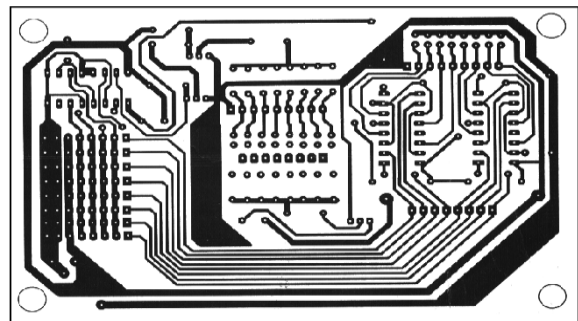
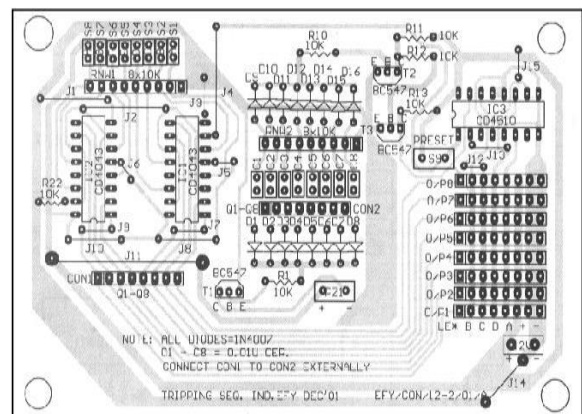


Fig 8: Component Layout



9.0 Conclusion

This paper is very useful for the safety of the electrical power systems. In applications like power stations and continuous process control plants, this paper is used to trip faulty systems to prevent damages and ensure the overall safety of the personnel and machinery. Then it gives the faulty areas sequentially through the display systems. Looking at all the tripped units doesn't reveal the cause of failure. It is therefore very important to determine the sequence of events that have occurred in order to exactly trace out the cause of failure and revive the system with minimal loss of time. It also helps in the protection of the electrical equipment from the over voltage and under voltage faults. It's necessary because these days over voltage and under voltage faults are very common in electrical power systems; therefore a protection is required for the safety of the electrical equipment. outage that occurred on the western interconnection.

References

- [1] J. C. Tan, P. A. Crossley, D. Kirschen, J. Goody, J. A. Downes, "An expert system for the back-up protection of a transmission network", IEEE Trans. Power Delivery, pp.508 -514 2000
- [2] J. C. Tan, P. A. Crossley, D. Kirschen, J. Goody J. A. Downes, "Fault section identification on a transmission network using action factors and expert system technology", Proc. 13th Power System Computation Conf., pp.820 – 826.
- [3] J. C. Tan, P. A. Crossley, I. Hall, J. Farrell, and P. Gale, "Evaluation of uncertainties in the back-up protection expert system", Proc. 2000 IEEE Power Engineering Soc. Summer Meeting, 2000
- [4] T. Saengsuwan, P. A. Crossley, C. Fernandez, "Expert systems applied to the back-up protection of a transmission network", Int. J. Eng. Intell. Syst. Elect Eng. Commun., 4(1), pp.43 -48 1996
- [5] Western Systems Coordinating Council disturbance report: For the power system outage that occurred on the western interconnection.
- [6] Western Systems Coordinating Council disturbance report: for the power system [7] S. Glover, Power System Analysis, Design, 1994: PWS
- [8] J. Burger, "The utility initiative for interoperability between intelligent electronic devices in the substation & mdash, Goals and status", Proc. 1999 IEEE PES SummerMeeting, pp.28 -31
- [9] Clinard, "GOMSFE (generic object models for substation and feeder equipment) models of multifunctional microprocessor relays", Proc. 1999 IEEE PES Summer Meeting, pp.38 -4